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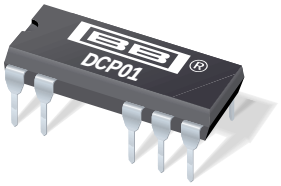


DCP0105

Miniature 5V Input, 1W Isolated DC/DC CONVERTER

FEATURES

- STANDARD JEDEC PLASTIC PACKAGE
- LOW PROFILE: 0.15" (3.8mm)
- SYNCHRONIZABLE
- OUTPUT SHORT CIRCUIT PROTECTION
- THERMAL SHUTDOWN
- EFFICIENCY: 70% AT FULL LOAD
- 1000Vrms ISOLATION
- 400kHz SWITCHING

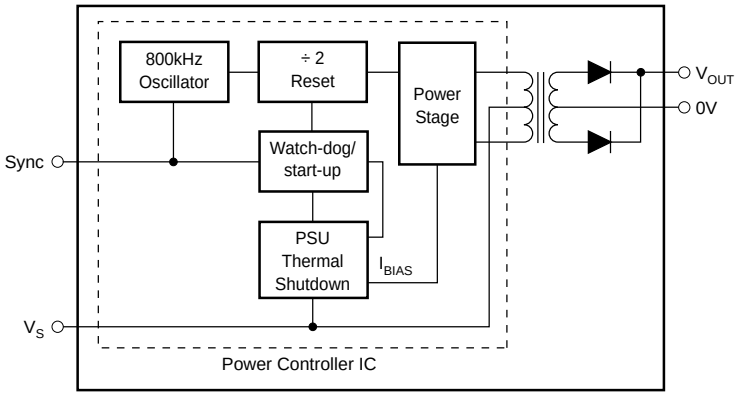
APPLICATIONS

- POINT OF USE POWER CONVERSION
- DIGITAL INTERFACE POWER
- GROUND LOOP ELIMINATION
- DATA ACQUISITION
- INDUSTRIAL CONTROL AND INSTRUMENTATION
- TEST EQUIPMENT

DESCRIPTION

The DCP0105 family is a series of high efficiency, 5V input isolated DC/DC converters. The 5V output DCP010505 is the first member of the family. In addition to 1W nominal galvanically isolated output power capability, the range of DC/DCs are also fully synchronizable. The devices feature thermal shutdown, and overload protection is implemented via watchdog circuitry. Advanced power-on reset techniques give superior reset performance and the devices will start into any load up to full power output.

The DCP01 family is implemented in standard-molded IC packaging, giving outlines suitable for high volume assembly.



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SPECIFICATIONS (Common)

At T_A = +25°C, V_{OUT} nominal (V_{NOM}) = +5V, and V_S = +5V, unless otherwise specified.

PARAMETER	CONDITIONS	DCP0105 MIN	DCP0105 TYP	DCP0105 MAX	UNITS
OUTPUT					
Power	V_{NOM} –10%		1		W
V_{NOM} vs Temperature			0.08		%/°C
Short Circuit Duration	V_S ±10%	No Limit			
INPUT					
Voltage Range		–10		10	%
Ripple Current	C_{IN} = I/P Capacitor = 1µF		42		mA
REGULATION					
Load Regulation	75% to 100% Load	–11			%
	75% to 10% Load			20	%
ISOLATION					
Rated Voltage	1s Test	1			kVrms
Insulation Resistance			>1		GΩ
SWITCHING/SYNCHRONIZATION					
Oscillator Frequency (F_{OSC})	Switching Frequency = F_{OSC}/2	720	800	880	kHz
Sync Input Low		0		0.8	V
Sync Input Current	V_{SYNC} = +2V		48		µA
Reset Time			3.8		µs
GENERAL					
Quiescent Current	No Load		15	40	mA
WEIGHT	14-pin DIP		1.08		g
TEMPERATURE RANGE					
Operating		–40		100	°C

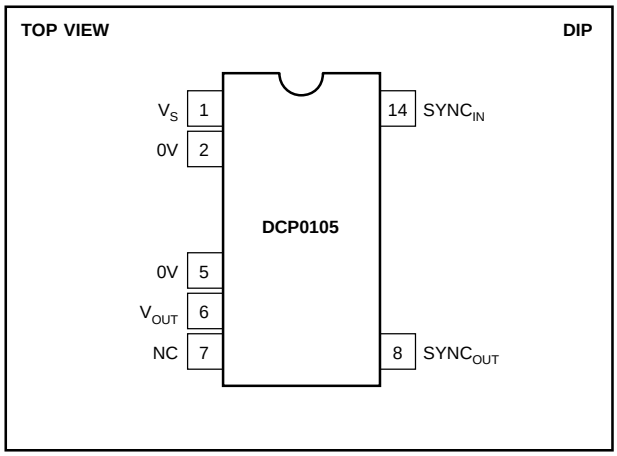
SPECIFICATIONS (DCP010505 Specific)

At T_A = +25°C, V_{OUT} nominal (V_{NOM}) = +5V, and V_S = +5V, unless otherwise specified.

PARAMETER	CONDITIONS	DCP010505 MIN	DCP010505 TYP	DCP010505 MAX	UNITS
OUTPUT					
Voltage (V_{NOM})	75% Full Load	4.75	5	5.15	V
Noise and Ripple	C_L = O/P Capacitor = 10µF		20		mVp-p
INPUT					
Supply Current	Full Load		240		mA
REGULATION					
Line Regulation	75% Full Load		1.003		%/1% of V_S
EFFICIENCY					
Efficiency	100% Load		70		%
	10% Load		52		%
Input/Output Capacitance			2.5		pF
TEMPERATURE					
Thermal Shutdown	Die Temperature	115		140	°C

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

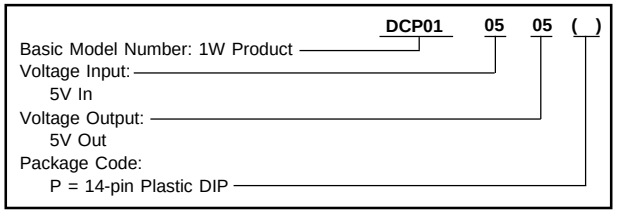
Input Voltage	7V
Storage Temperature	–60°C to +150°C
Lead Temperature (soldering, 10s)	300°C

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
DCP010505P	14-Pin Dual In-Line Plastic	010-1

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION



PIN DEFINITION

PIN #	PIN NAME	DESCRIPTION
1	V_S	Voltage Input.
2	0V	Input Side Common.
5	0V	Output Side Common.
6	V_{OUT}	Voltage Out.
7	NC	Not Connected.
8	$SYNC_{OUT}$	Unregulated 400kHz Output from Transformer.
14	$SYNC_{IN}$	Synchronize Pin.

ELECTROSTATIC DISCHARGE SENSITIVITY

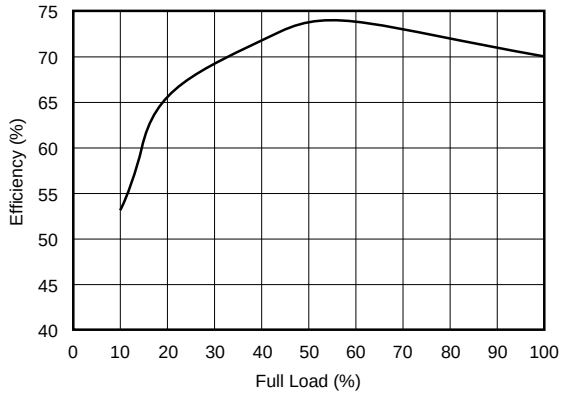
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

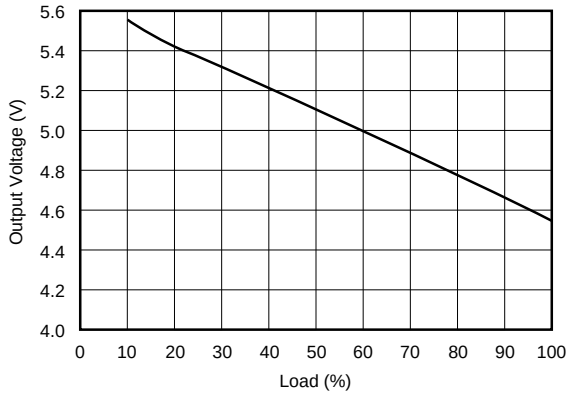
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, unless otherwise noted.

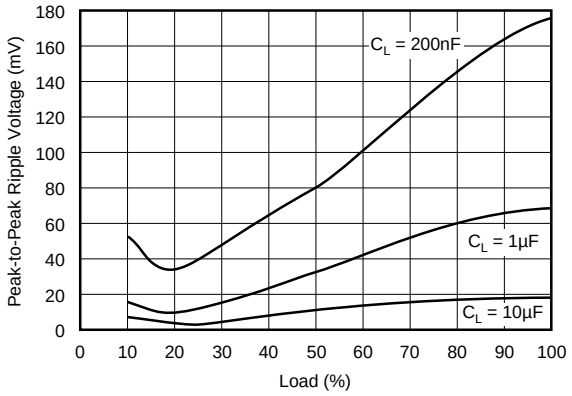
EFFICIENCY vs LOAD



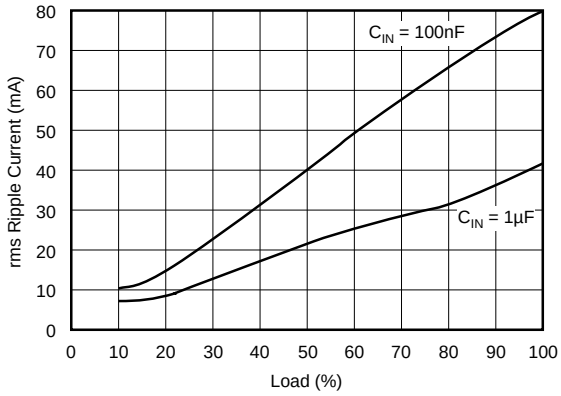
OUTPUT VOLTAGE vs LOAD



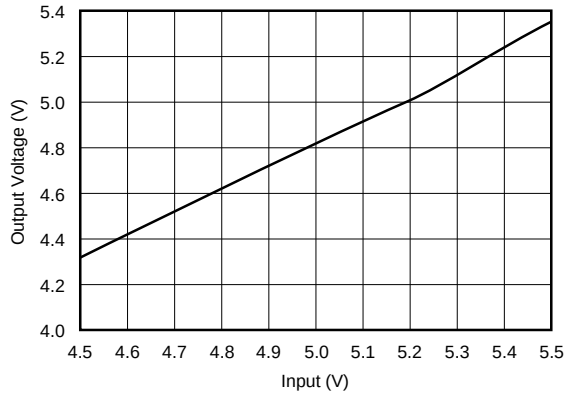
PEAK-TO-PEAK RIPPLE VOLTAGE vs LOAD



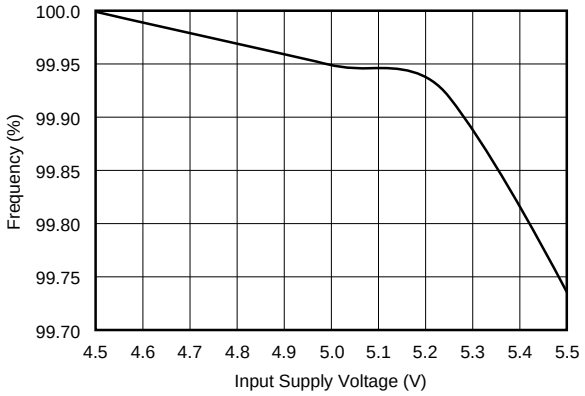
RMS RIPPLE CURRENT vs LOAD



OUTPUT vs INPUT VOLTAGE



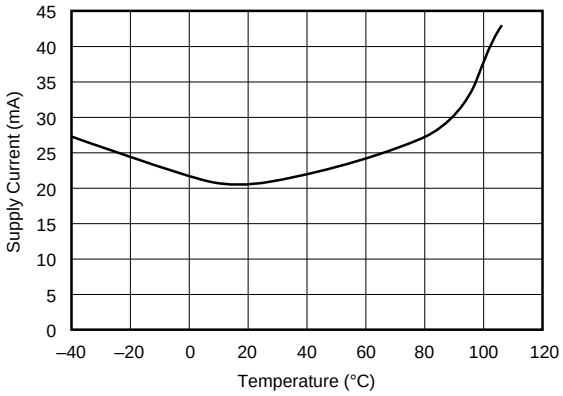
SWITCHING FREQUENCY vs SUPPLY VOLTAGE



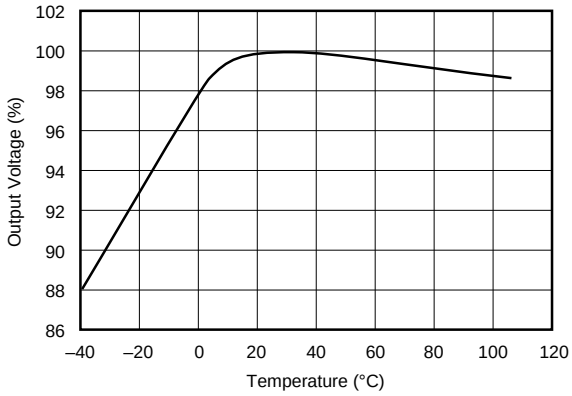
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, unless otherwise noted.

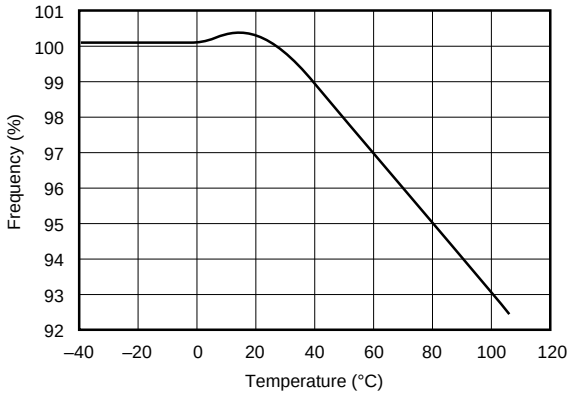
QUIESCENT CURRENT vs TEMPERATURE



OUTPUT VOLTAGE vs TEMPERATURE



SWITCHING FREQUENCY vs TEMPERATURE



FUNCTIONAL DESCRIPTION

OVERVIEW

The DCP0105 offers 1W of unregulated output power from a 5V input source with a typical efficiency of 70%. This is achieved through highly integrated packaging technology and the implementation of a custom power stage and control IC.

POWER STAGE

This uses a pull-pull, center-tapped topology switching at 400kHz (divide by 2 from 800kHz oscillator).

OSCILLATOR AND WATCHDOG

The on-board 800kHz oscillator provides the switching frequency via a divide by 2 and allows synchronization via the $SYNC_{IN}$ pins. To synchronize any number of DCP0105 family of devices, simply tie the $SYNC_{IN}$ pins together (see the Synchronization section.) The patented(1) watchdog circuitry protects the DC/DC against a stopped oscillator. It checks the oscillator frequency which, if drops below a threshold, will shut down the output stage, i.e., it will be tri-stated after approximately 10µs.

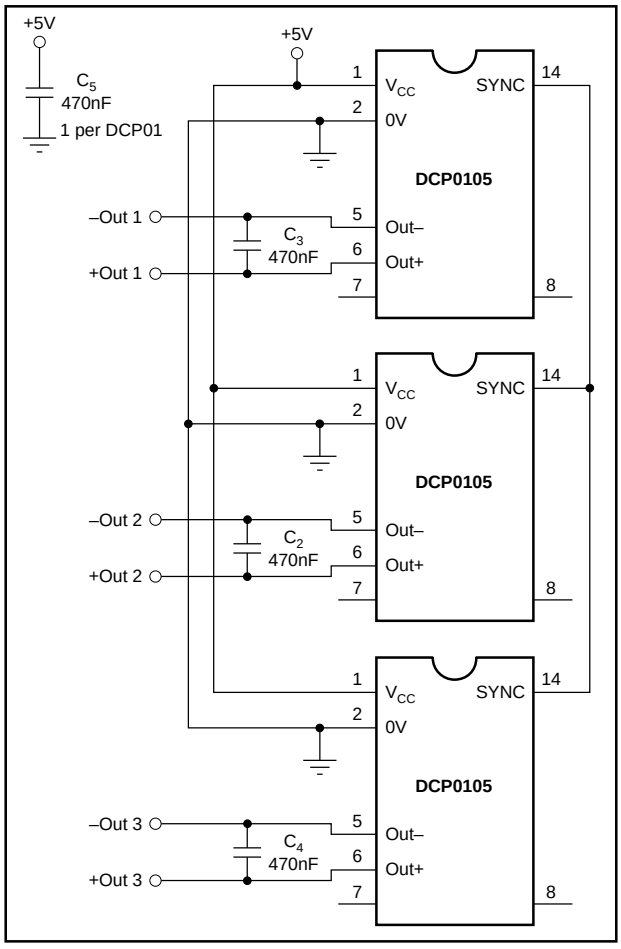


FIGURE 1. Standard Interface.

THERMAL SHUTDOWN

The DCP0105 is also protected further by implementing thermal shutdown. If the on-chip temperature reaches a predetermined value, the DC/DC will shutdown. This effectively gives indefinite short circuit protection for the DC/DC. The on-board bandgap reference is also used to bias the power stage.

SYNCHRONIZATION

Any number of DCP0105 devices can be synchronized by connecting the $SYNC_{IN}$ pins on the devices together (see Figure 1). All the DCP0105 devices will then self-synchronize.

This same synchronization method will apply to other V_{IN} versions of the DCP01 family, allowing synchronization of various V_{OUT} and V_{IN} DC/DCs.

The $SYNC_{OUT}$ pin gives an unrectified 400kHz signal from the transformer. This can be used to set the timing of external circuitry on the output side.

DIVIDE BY 2 RESET

Isolated DC/DC converter performance normally suffers after power reset. This is because a change in the steady state transformer flux creates an offset after power-up. The DCP01 family does not suffer from this problem. This is achieved through a patented(1) technique employed on the divide by 2 reset circuitry resulting in no change in output phase after power interruption.

CONSTRUCTION

The DCP0105's basic construction is the same as standard ICs. There is no substrate within the molded package. The DCP0105 is constructed using an IC, Shottky diodes, and a wound magnetic toroid on a leadframe. As there is no solder within the package, the DCP0105 does not require any special PCB assembly processing. This results in an isolated DC/DC with inherently high reliability.

ADDITIONAL FUNCTIONS

DISABLE/ENABLE

The DCP0105 can be disabled or enabled by driving the $SYNC_{IN}$ pin with an open drain CMOS gate. If the gate is pulled low then the DCP0105 will disable. The disable time depends on the output loading but the internal shutdown takes 10µs. Making the gate open drain will re-enable the DCP0105. However, there is a trade-off in using this function; the DCP0105 quiescent current may increase and the on-chip oscillator may run slower. This degradation in performance is dependent on the external CMOS gate capacitance, therefore the smaller the capacitance, the lower the performance degrease. Driving the $SYNC_{IN}$ pin with a CPU type tri-state output, which has a low output capacitance, offers the lowest reduction in performance.

NOTE: (1) Patents pending.

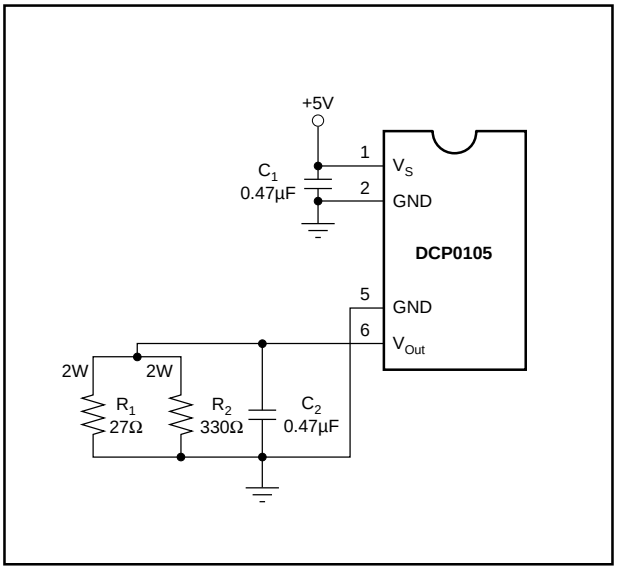


FIGURE 2. DCP0105 Fully Loaded.

DECOUPLING

Ripple Reduction

It is recommended that at least a 0.1µF capacitor is used to decouple V_S. In Figure 2 where the DCP0105 is shown fully loaded, there are 0.47µF capacitors on V_S and V_{OUT} to give good ripple reduction.

EXTERNAL SYNCHRONIZATION

The DCP0105 can be synchronized externally if required using a simple external interface. Figure 3 shows a universal interface using a 4066 quad switch. The CTL and $SYNC_{ON}$ pins are used to select external synchronization or self-synchronization.

This interface can also be used to stop (disable) the DCP0105.

CTL	$SYNC_{ON}$	FUNCTION
1	1	External Sync
—	0	Self-Sync
0	1	Device Stop

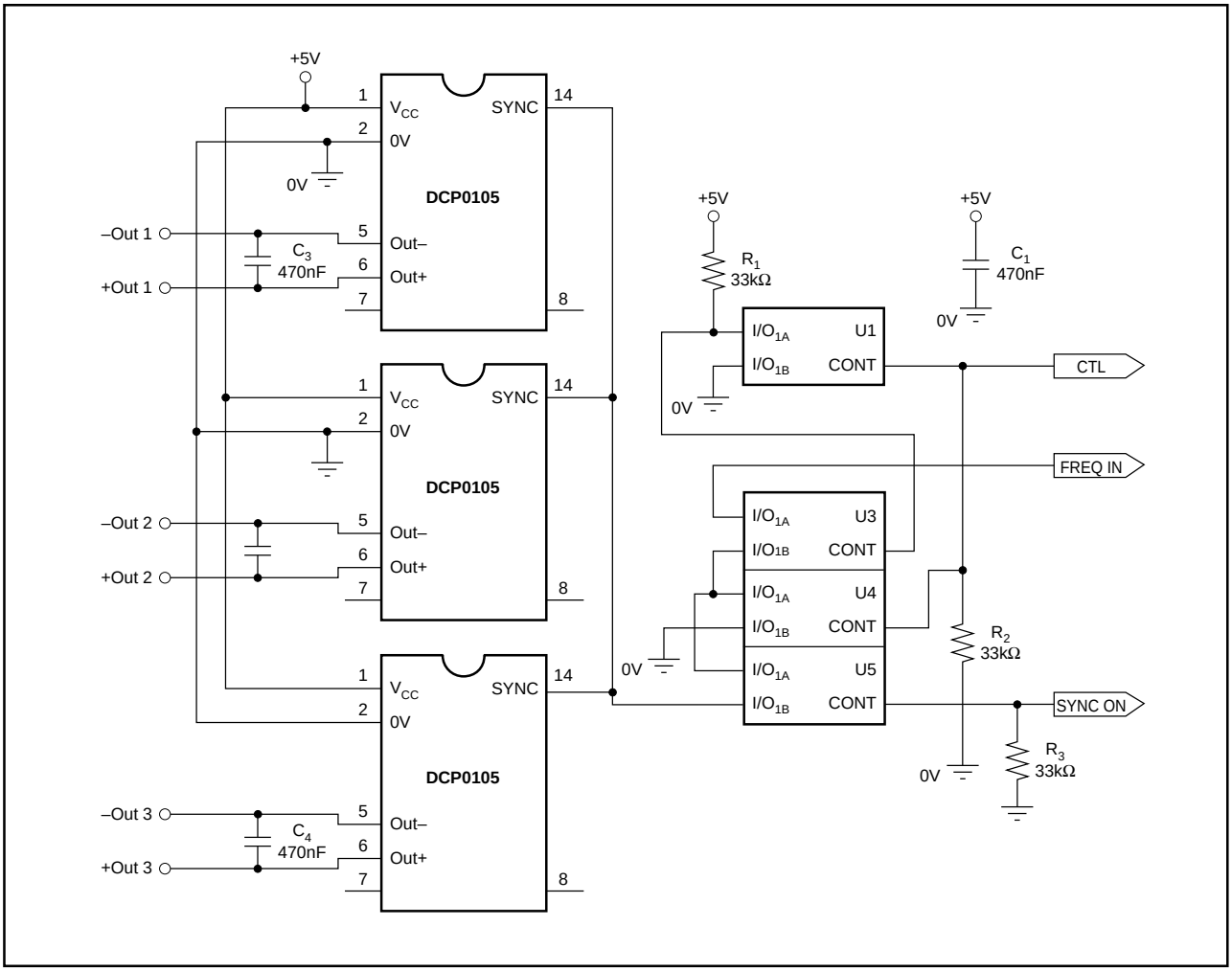


FIGURE 3. Universal Interface.

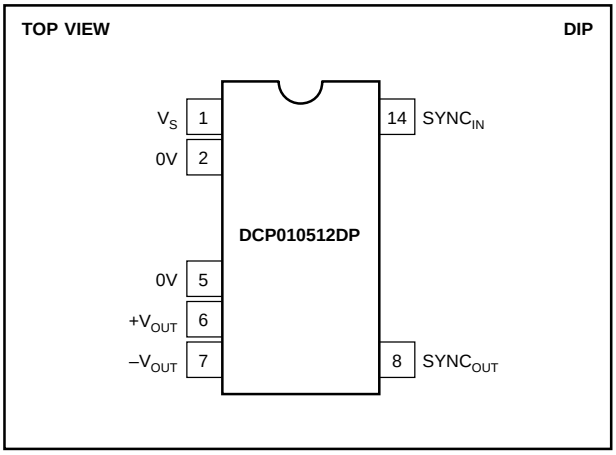
DCP0105 ADDENDUM

SPECIFICATIONS (DCP010512DP)

At T_A = +25°C, V_{OUT} nominal (V_{NOM}) = ±12V, and V_S = +5V, unless otherwise specified.

PARAMETER	CONDITIONS	DCP010512			UNITS
		MIN	TYP	MAX	
OUTPUT					
Voltage (V_{NOM})	75% Full Load	±11.4	±12	±12.6	V
Noise and Ripple	C_L = O/P Capacitor = 10µF		20		mVp-p
INPUT					
Supply Current	Full Load		240		mA
REGULATION					
Load Regulation	100% to 75% Load		7	10	%
	75% to 25% Load		12	16	%
	25% to 10% Load		7	11	%
Line Regulation	75% Full Load		1.003		%/1% of V_S
EFFICIENCY					
Efficiency	100% Load		72		%
	10% Load		36		%
Input/Output Capacitance			2.5		pF
TEMPERATURE					
Thermal Shutdown	Die Temperature	115		140	°C
QUIESCENT CURRENT					
Quiescent Current			33		mA

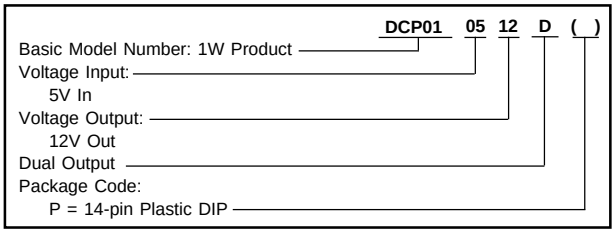
PIN CONFIGURATION



PIN DEFINITION

PIN #	PIN NAME	DESCRIPTION
1	V_S	Voltage Input.
2	0V	Input Side Common.
5	0V	Output Side Common.
6	$+V_{OUT}$	+Voltage Out.
7	$-V_{OUT}$	–Voltage Out.
8	$SYNC_{OUT}$	Unregulated 400kHz Output from Transformer.
14	$SYNC_{IN}$	Synchronize Pin.

ORDERING INFORMATION



ADDITIONAL INFORMATION

RIPPLE REDUCTION

It is recommended that at least 0.1µF capacitors are used on the outputs to reduce ripple. Connecting 0.47µF capacitors from $+V_{OUT}$ and $-V_{OUT}$ to 0V (pin 5) close to the DC/DC will give good ripple reduction.

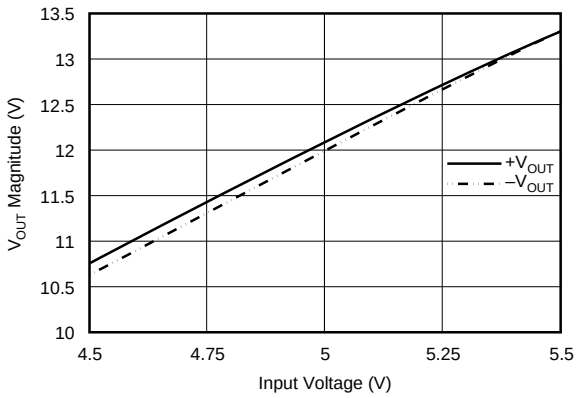
SINGLE OUT OPERATION

As the DCP010512DP has floating outputs, it can be configured for +24V output or –24V output by connecting pin 7 ($-V_{OUT}$) or pin 6 ($+V_{OUT}$) respectively to the output side system common. It is still necessary to connect the two ripple reduction capacitors to pin 5.

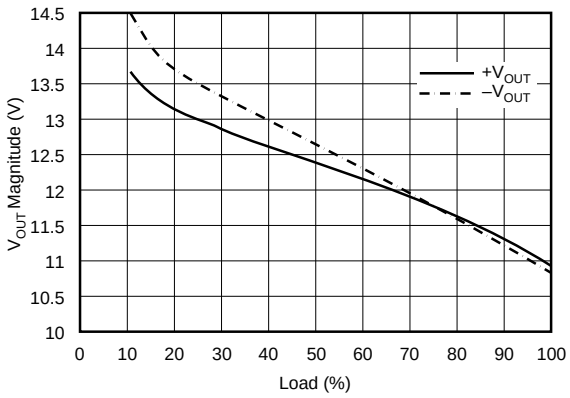
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_{OUT} nominal (V_{NOM}) = ±12V, and V_S = +5V, unless otherwise specified.

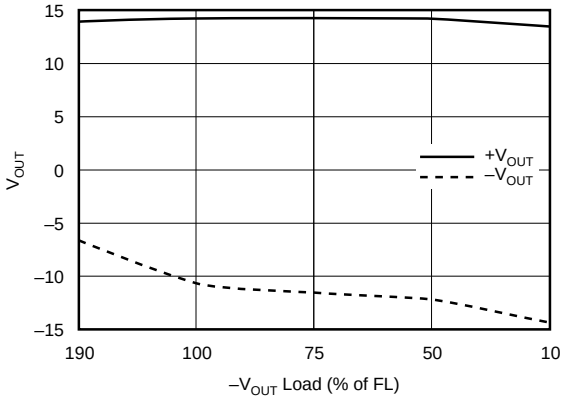
OUTPUT vs INPUT VOLTAGE



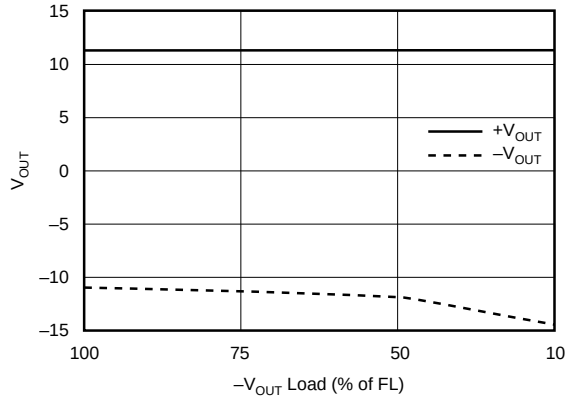
OUTPUT VOLTAGE vs LOAD



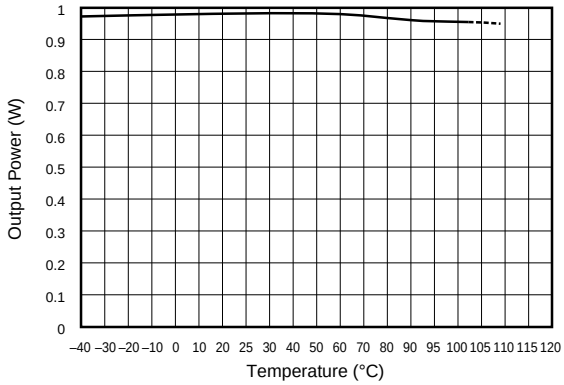
LOAD BALANCE (+V_{OUT} Load = 10%)



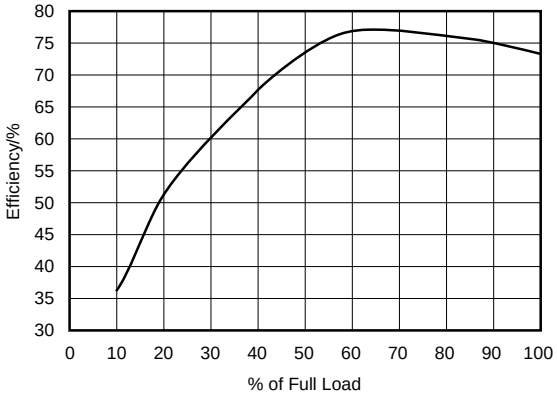
LOAD BALANCE (+V_{OUT} Load = 100%)



OUTPUT POWER vs TEMPERATURE



EFFICIENCY vs LOAD



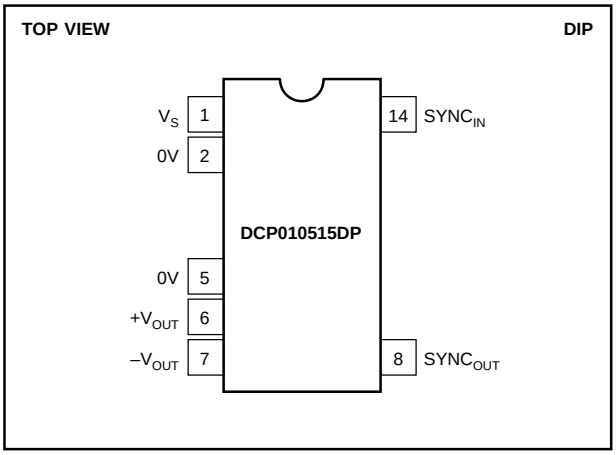
DCP0105 ADDENDUM

SPECIFICATIONS (DCP010515DP)

At T_A = +25°C, V_{OUT} nominal (V_{NOM}) = ±15V, and V_S = +5V, unless otherwise specified.

PARAMETER	CONDITIONS	DCP010515 MIN	DCP010515 TYP	DCP010515 MAX	UNITS
OUTPUT					
Voltage (V_{NOM})	75% Full Load	±14.25	±15	±15.75	V
Noise and Ripple	C_L = O/P Capacitor = 10µF		20		mVp-p
INPUT					
Supply Current	Full Load		240		mA
REGULATION					
Load Regulation	100% to 75% Load		7	10	%
	75% to 25% Load		12	16	%
	25% to 10% Load		11	15	%
Line Regulation	75% Full Load		1.003		%/1% of V_S
EFFICIENCY					
Efficiency	100% Load		75		%
	10% Load		39		%
Input/Output Capacitance			2.5		pF
TEMPERATURE					
Thermal Shutdown	Die Temperature	115		140	°C
QUIESCENT CURRENT					
Quiescent Current			34		mA

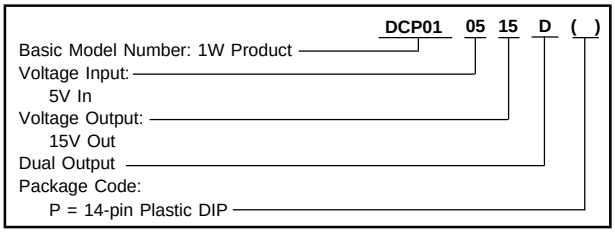
PIN CONFIGURATION



PIN DEFINITION

PIN #	PIN NAME	DESCRIPTION
1	V_S	Voltage Input.
2	0V	Input Side Common.
5	0V	Output Side Common.
6	$+V_{OUT}$	+Voltage Out.
7	$-V_{OUT}$	–Voltage Out.
8	$SYNC_{OUT}$	Unregulated 400kHz Output from Transformer.
14	$SYNC_{IN}$	Synchronize Pin.

ORDERING INFORMATION



ADDITIONAL INFORMATION

RIPPLE REDUCTION

It is recommended that at least 0.1µF capacitors are used on the outputs to reduce ripple. Connecting 0.47µF capacitors from $+V_{OUT}$ and $-V_{OUT}$ to 0V (pin 5) close to the DC/DC will give good ripple reduction.

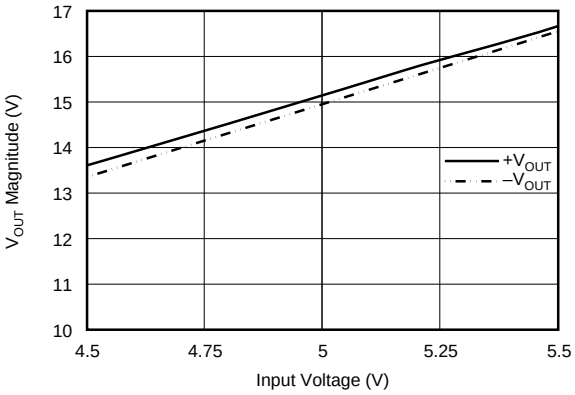
SINGLE OUT OPERATION

As the DCP010515DP has floating outputs, it can be configured for +30V output or –30V output by connecting pin 7 ($-V_{OUT}$) or pin 6 ($+V_{OUT}$) respectively to the output side system common. It is still necessary to connect the two ripple reduction capacitors to pin 5.

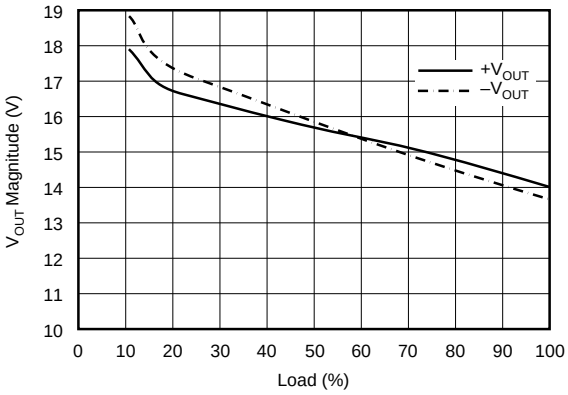
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_{OUT} nominal (V_{NOM}) = ±15V, and V_S = +5V, unless otherwise specified.

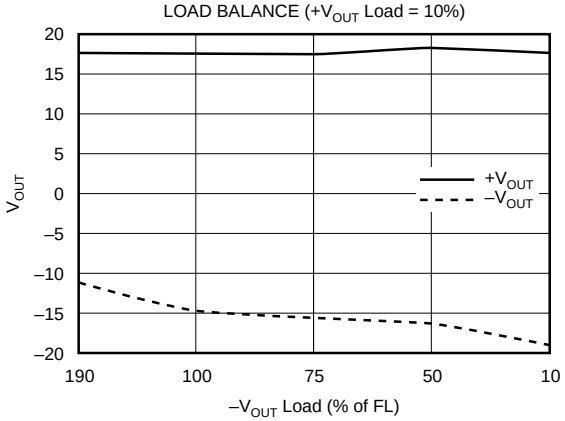
OUTPUT vs INPUT VOLTAGE



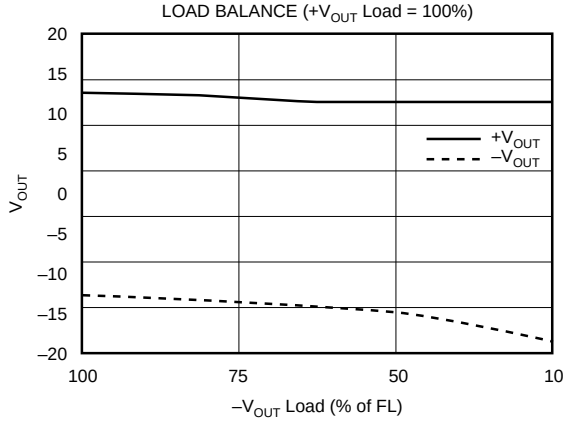
OUTPUT VOLTAGE vs LOAD



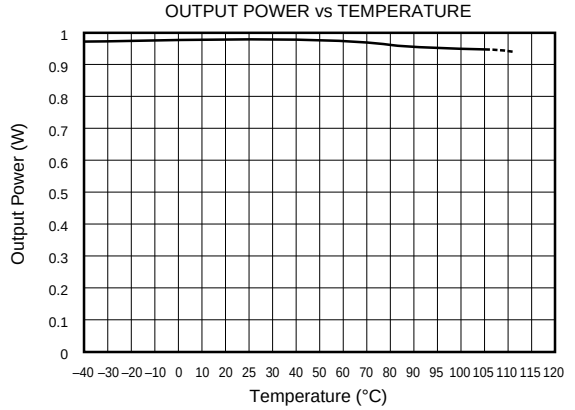
LOAD BALANCE (+V_{OUT} Load = 10%)



LOAD BALANCE (+V_{OUT} Load = 100%)



OUTPUT POWER vs TEMPERATURE



EFFICIENCY vs LOAD